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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/613,653	07/03/2003	Paul A. LaBerge	6909.01	7250

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Devan V. Padmanabhan
DORSEY & WHITNEY LLP
Intellectual Property Department
50 South Sixth Street, Suite 1500
Minneapolis, MN 55402-1498

EXAMINER	
SIEK, VUTHE	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 08/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/613,653	LABERGE, PAUL A.	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *20-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *20-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/613,653 and amendment filed on 6/12/2006. Claims 20-27 remain pending in the application.

Terminal Disclaimer

2. The terminal disclaimer filed on 6/12/06 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of the patents 6,209,119 and 6,601,228 has been reviewed and is accepted. The terminal disclaimers have been recorded.

Correction of Amendment (June 12, 2006)

3. The amendment filed on June 12, 2006 has been correct as --Claim 28 is canceled--, on page 5 of the amendment, instead of "Claim 29".

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 20-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Tavana et al. (5,825,202).

6. As to claim 20, Tavana et al. teach a process for use in manufacturing of application specific integrated circuits (manufacturing circuits shown in Fig. 2), comprising providing a semi-fabricated semiconductor wafer that lacks a metal one layer and on which has been formed a plurality of circuits that comprise a logic design and at least one programmable circuit capable of performing at least one of a plurality of logic transfer functions upon programming (Fig. 2 comprising a logic design (ASLA 14 & FPGA 12 and at least one programmable circuit (FPGA 12), where FPGA 12 comprising control logic blocks that can be programmed and reprogrammable to provide a plurality of logic functions; ICs shown in Fig. 2 allows for post-fabrication design modification, accelerated modification of the FPGA portion, combined with the decreased cost of the mask-defined portion as described in col. 3 lines 7-43); determining modifications to the logic design that are desired by examining an original specimen of the application specific integrated circuits (ICs Fig. 2) with a metal one layer (mask-defined or other permanent custom chip architecture; see col. 3 lines 7-43; col. 5 lines 5564; col. 6 lines 34-64. In order to perform design modifications of ICs shown in Fig. 2, designers must analyze and examine an original specimen of ICs with a metal one layer to determine connections. Tavana et al. also teach determining desired changes in the metal one layer needed to implement to modifications in logic design, including connecting the at least one programmable circuit (programmable logic blocks in FPGA of Fig. 2) to the plurality of circuits (see design modifications of ICs Fig. 2 including their connections in Fig. 3, 4, 5, 6, 7; post-fabrication design modifications; col. 3 lines 7-67); and forming a metal one layer on said semi-fabricated semiconductor wafer different from the metal

layer of original specimen to effect the desired changes (Tavana et al. teach post-fabrication design modifications; col. 3 lines 6-67; col. 4 lines 1-19). It is noted that the mask-defined of ASLA include metal one layer that different from metal one layer that is used to perform connections of programmable logic blocks in FPGA to provide a plurality of functions).

7. As to claim 21, Tavana et al. teach ICs shown in Fig. 2 comprise interconnecting the plurality of circuits by integrated circuit connection circuitry (interconnect cells A, B C for interconnect between circuits FPGA and circuits in ASLAs) and connecting the at least one programmable circuit (programmable circuits in FPGA) to the integrated circuit connection circuitry (see Fig. 5).

8. As to claims 22-23 and 26, FPGA used in ICs shown in Fig. 1 & 2 is one of Xilinx field programmable devices that can be programmed and reprogrammed by loading memory cells (configuration register) in the configuration structure to determine what logic function will be applied by the control logic blocks to signals on its input leads to generate a signal on its output lead or leads (col. 2 lines 34-48; col. 5 lines 30-54). ICs shown in Fig. 2 include FPGA and ASLAs that are allowed for post-fabricated design modifications, accelerated modification of the FPGA portion, combined with the decreased cost of the mask-defined portion (Col. 3 lines 40-43).

9. As to claims 24 and 27, Tavana et al. teach FPGA including a plurality of control logic blocks that are programmable and reprogrammable (col. 5 lines 30-54). Fig. 1 and 2 show dispersed pattern of the control logic blocks on the wafer to allow for post-

fabricated design modifications, accelerated modification of the FPGA portion, combined with the decreased cost of the mask-defined portion (col. 3 lines 7-43).

10. As to claim 25, Tavana et al. teach the act of determining whether modifications to the logic design are desired comprising testing a semiconductor wafer upon which the plurality of circuits have been interconnected by integrated circuitry connection circuitry (interconnect cells A, B, C shown in Fig. 2) (see col. 3 lines 7-62).

Remarks

11. Based on the amended claims, Examiner submits new ground of rejection to Tavana et al. The patent to Tavana et al. teaches every claimed limitation as recited.

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek

VUTHE SIEK
PRIMARY EXAMINER